CML Semiconductor Products

PRODUCT INFORMATION

FX406 Unifil™ Universal Analogue Signal Processor

Publication D/406/7 July 1994

Features/Applications

- 2nd Order Multiple Filter
- PLL Clock Generator
- Programmable Q
- F_c set by RC or External Clock
- Gain Adjustment on Inputs
- Single 5 Volt Supply CMOS
- Programmable Filters
- Voltage Controlled Filters
- Sinewave Oscillator
- Tracking Filters/Oscillators
- FSK and PSK Modems
- Square-Sine, Pulse-Sine Converter

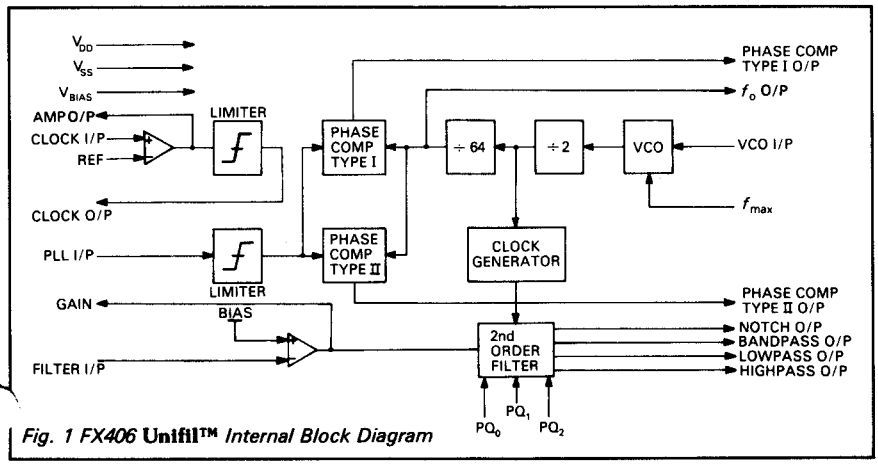


Fig. 1 FX406 **Unifil™** *Internal Block Diagram*

FX406

Brief Description

The FX406 **Unifil™** is a CMOS LSI circuit with a wide variety of signal processing applications. The device consists of a switched capacitor second order active filter with a single input and outputs for bandpass, notch, lowpass and highpass frequency responses, together with a clock generator to provide the switched capacitor sampling clock frequency. The centre frequency of the bandpass and notch filters is the same as the cut-off frequency f_c of the lowpass and highpass filters. The filter sampling clock is derived from a multiplying phase locked loop whose reference or input frequency is the same as the desired cut-off frequency of the filters. The PLL comprises a voltage controlled oscillator, one of two types of phase comparator, a fixed divider and an external RC loop filter. Facilities are provided to programme the cut-off frequency of the filters by injecting an external signal into the PLL, or by using the on-chip clock oscillator circuit. The filters have gain adjustment on the input and the Q is programmable to eight values between 0.54 and 8.0.

Pin Number / Function

FX406J	FX406LG	Function
1	1	**PCI O/P:** Output of 'EXCLUSIVE-OR' type phase comparator. See Note on PLL operation.
2	2	**PLL I/P:** Input to limiter preceding phase comparators.
3	4	**f_o O/P:** Divided down VCO square wave output.
4	5	**PQ_2 I/P:** These pins set the Q of the filters; they have internal resistors to
5	6	**PQ_0 I/P:** set Q = 0.71 if left open circuit (logic state 1 0 1, = 1MΩ)
6	7	**PQ_1 I/P:** Possible Q values are:

PQ_2	PQ_1	PQ_0	Q	
1	1	1	0.54*	
1	1	0	0.58	(Bessel)
1	0	1	0.71	(Butterworth)
1	0	0	1.00	
0	1	1	1.31	
0	1	0	2.00	
0	0	1	4.00	
0	0	0	8.00	

* (Cascaded with a 1.31 section for a 4th order Butterworth filter).

7	8	**Clock O/P:** Digital output of limiter from uncommitted amplifier.
8	10	**Amp O/P:** Analogue output of uncommitted amplifier.
9	11	**Reference:** Inverting input to uncommitted amplifier.
10	12	**Clock I/P:** Non-inverting input to uncommitted amplifier.
11	13	**V_{SS} :** Negative supply.
12	14	**V_{BIAS} :** $V_{DD}/2$ bias pin, externally decoupled.
13	15	**Filter I/P:** Input to filter input buffer amplifier.
14	16	**Gain:** Output of filter input buffer amplifier.
15	17	**Highpass O/P:** Output of the highpass filter. The cut-off frequency is identical to the input frequency of the PLL when locked.
16	18	**Lowpass O/P:** Output of the lowpass filter. The cut-off frequency is the same as the highpass filter.
17	19	**Bandpass O/P:** Output of the bandpass filter. f_O is identical to the input frequency to the PLL when locked. Gain in passband is dependent on Q.
18	20	**Notch O/P:** Output of the notch filter, f_O, is the same as the bandpass filter.
19	21	**VCO I/P:** Input of the VCO control voltage, usually connected to loop filter output.
20	22	**f_{MAX} :** This pin is connected to V_{SS} via an external resistor R_{MAX} (R_{MAX}, see Figure7). The value sets the maximum frequency of operation of the VCO, see Figures 9(a) and (b).
21	23	**PCII O/P:** Output of the edge-triggered type of phase comparator. See Note on PLL operation.
22	24	**V_{DD} :** Positive supply.
	3, 9	No Connection: Leave open circuit.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	FX406J	−30°C to + 85°C
	FX406LG	−30°C to + 70°C
Storage temperature range:	FX406J	−55°C to +125°C
	FX406LG	−40°C to + 85°C
Maximum device dissipation:		All versions 100mW

Operating Limits

Typical characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5V, T_{amb} = 25°C, PLL input = 1kHz, filter Q = 0.707.
Limits specified over the full operating temperature and working voltage range.

Characteristics	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply voltage		4.5	5.0	5.5	V
Supply current		—	4.5	8.5	mA
Input impedance (Filter & Clock Osc)		1.0	—	—	MΩ
Output impedance (Filter Outputs)		—	—	1.0	kΩ
Output impedance (Clock Output)		—	—	1.0	kΩ
Input impedance (PQ_0, PQ_1, PQ_2)		250	—	—	kΩ
Output impedance (f_o output)		—	—	5.0	kΩ
Input logic '1'		70% V_{DD}	—	—	V
Input logic '0'		—	—	30% V_{DD}	V
Filter Characteristics					
Maximum cutoff frequency		4.0	5.0	—	kHz
Minimum cutoff frequency		—	50	100	Hz
Gain at f_c (f_o) (HP BP LP)		—	20 log Q	—	dB
Notch filter depth	1	—	−30	—	dB
Notch accuracy	1	—	±0.5% f_o	—	Hz
Maximum signal handling	2	3.0	—	—	Vp-p
No signal filter noise (BP)		—	6.0	—	mVrms
(LP HP N)		—	3.0	—	mVrms
VCO Characteristics					
VCO maximum frequency	3	4.0	5.0	—	kHz
VCO minimum frequency	3	—	50	100	Hz
VCO input impedance		1.0	—	—	MΩ
Phase Comparator Characteristics					
Input impedance		100	500	—	kΩ
Input sensitivity	4	30	10	—	mVrms
Output impedance PCII	5	—	—	1.5	kΩ
PCI		—	—	1.5	kΩ
Amplifier Characteristics (Clock Oscillator and Filter inputs)					
Open loop gain		40	—	—	dB
Input offset voltage		—	—	10	mV
Maximum signal handling	2	3.0	—	—	Vp-p

Notes: *1. Q = 8.*
2. For SINAD = 30dB at output.
3. VCO frequency divided down at f_o output.
4. At PLL input pin, ac coupled.
5. Output impedance when conducting, output is high impedance three-state when PLL is in lock.

Typical Filter Frequency Responses

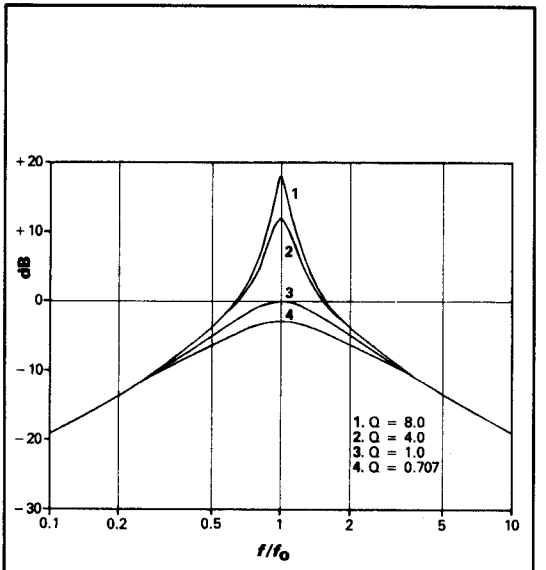


Fig. 2 Bandpass Frequency Response for different Q Values

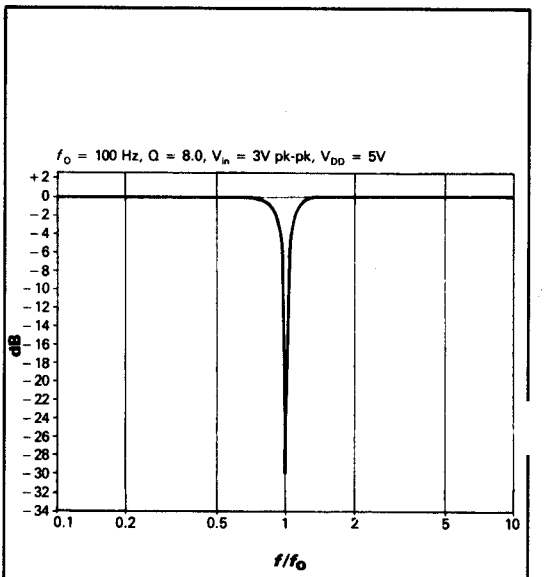


Fig. 3 Notch Frequency Response

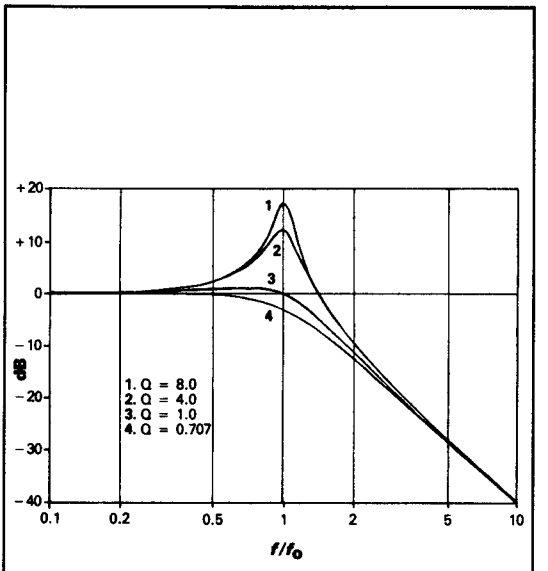


Fig. 4 Lowpass Frequency Response for different Q Values

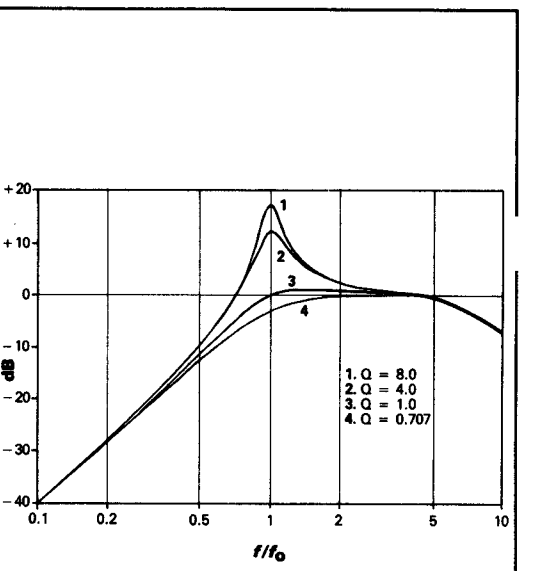


Fig. 5 Highpass Frequency Response for different Q Values

PC4060 PCB For Design Evaluation

To assist in customer's design evaluation of the FX406, a PCB is available to enable external components to be connected for easy evaluation of application circuits.

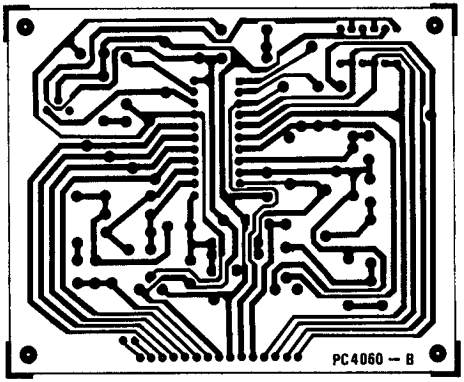


Fig. 6 (a) Track Side

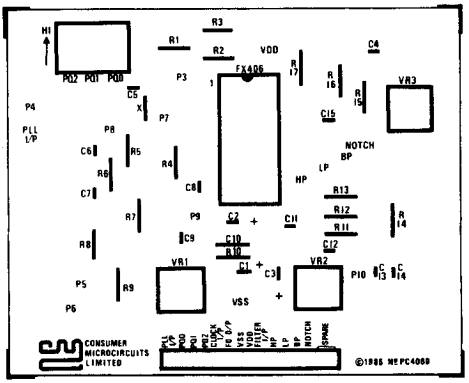


Fig. 6 (b) Component Side

Fig. 6 PC4060 Printed Circuit Board

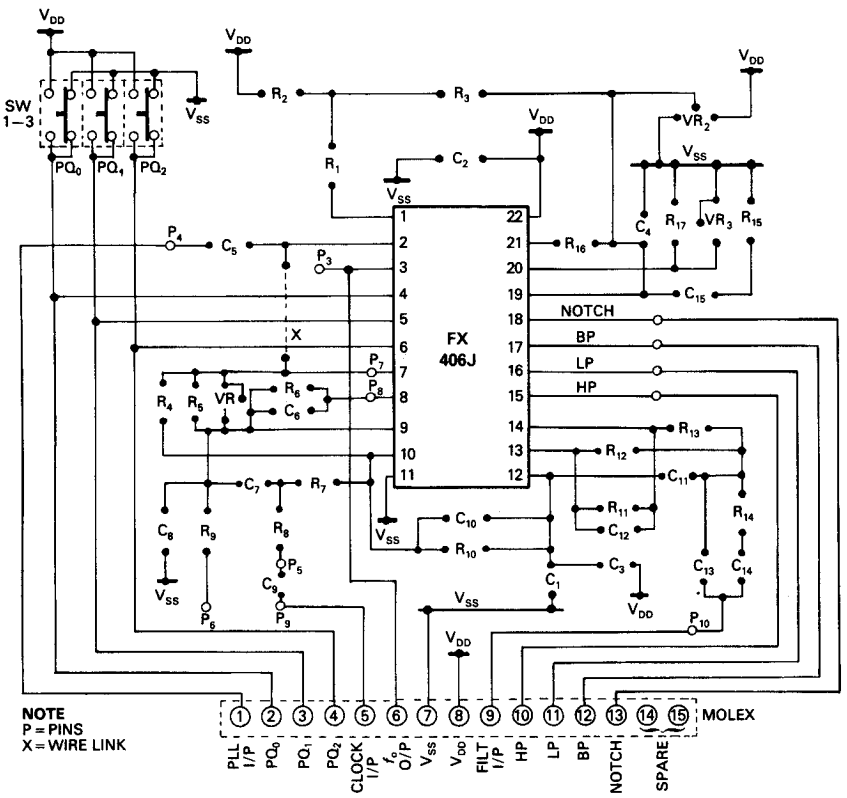


Fig. 6 (c) PC4060 Printed Circuit Board Schematic Diagram

External Component Connections

The following examples of external component connections illustrate the basic modes of operation of the FX406. Where component references are used, these are the same as the circuit references on the PC4060 Evaluation PCB.

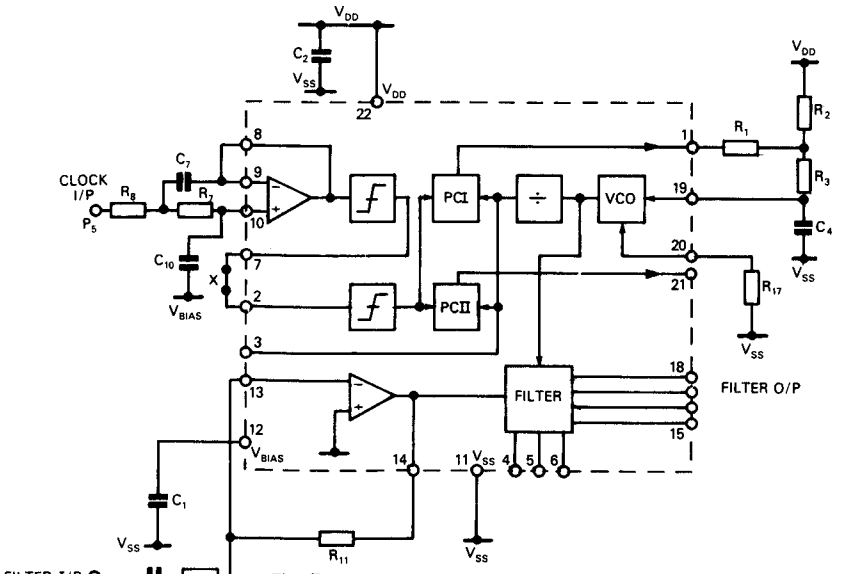


Fig. 7 Example 1

- —Using PCI with lag loop filter
- —VCO range set using R_{max} (R_{17}) and f_{min} potential divider (R_1, R_2)
- —Filter input with simple gain adjustment
- —Clock input pre-filtered with 2nd order LPF.

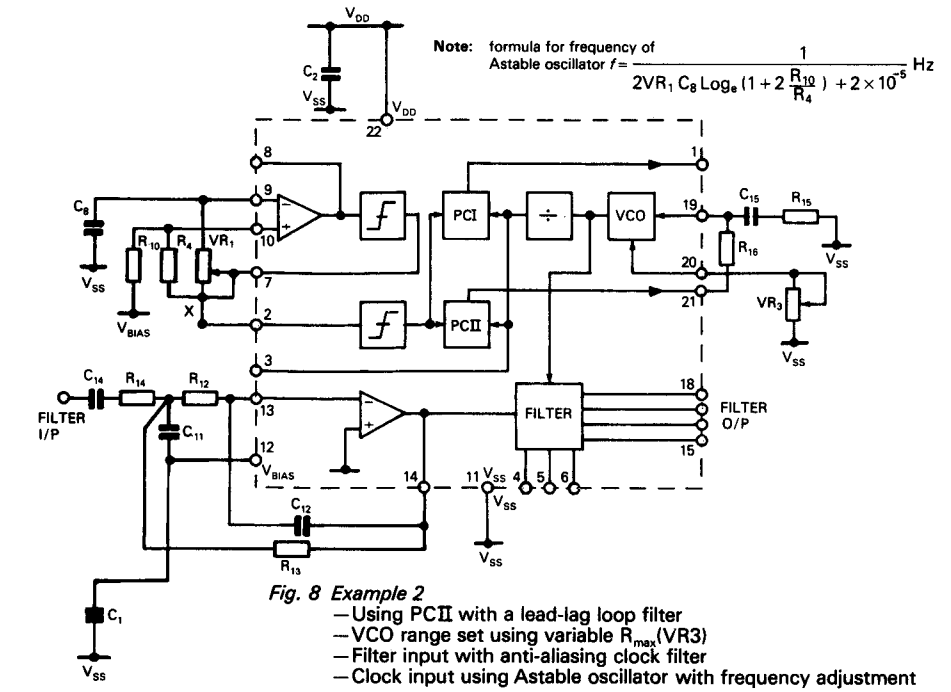


Fig. 8 Example 2

- —Using PCII with a lead-lag loop filter
- —VCO range set using variable R_{max}(VR3)
- —Filter input with anti-aliasing clock filter
- —Clock input using Astable oscillator with frequency adjustment

Application Notes

Note 1 — Setting VCO Frequency Range.

Set f_{max}* of VCO by selecting R_{max} using graph in Fig. 9(a) & 9(b). If Phase comparator I is being used, it is also possible to set f_{min} of the VCO by using the network shown in Fig. 9(c). R_{min} may be determined using the graph in Fig. 9(c).

*Frequencies shown in graphs are actually $f_{VCO}/128$.

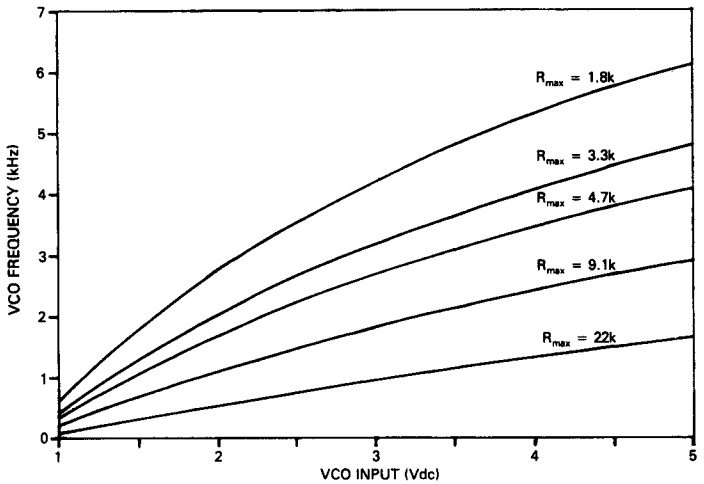


Fig. 9(a) VCO Conversion Gain Curves For Different Values of R_{max} (R_{17})

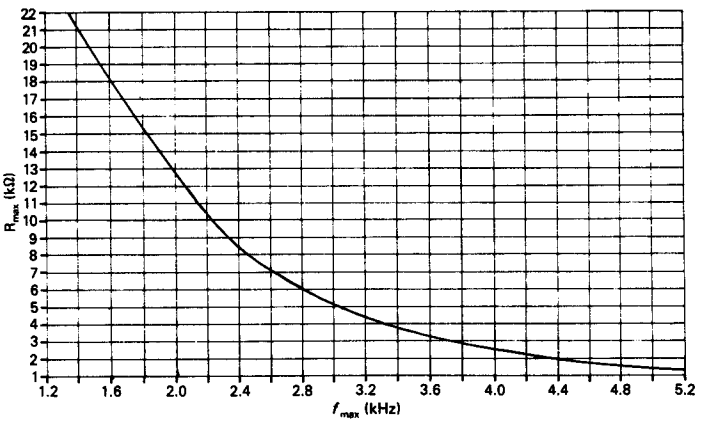


Fig. 9(b) VCO f_{max} Versus R_{max} Curve

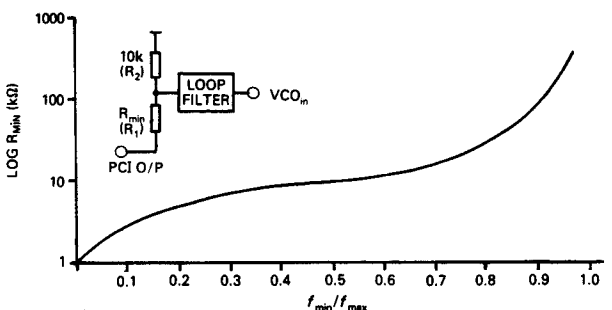


Fig. 9(c) R_{min} Versus Ratio f_{min}/f_{max}

Note 2 — Loop Filter Design

In order to maintain a fixed phase relationship between the VCO and reference input (or clock) signals, a 'second order loop' must be established. This is achieved by placing a lowpass filter between the phase comparator output and the VCO control input

This filter may be a 'lag' filter, (Fig.10a)or for improved stability a 'lead-lag' filter, (Fig10b).

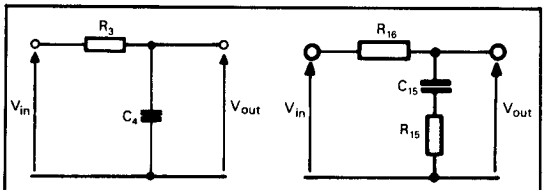


Fig. 10(a) 'Lag' Filter *Fig. 10(b) 'Lead-Lag' Filter*

The overall loop gain is given by $K_p . K_F \frac{K_{vco}}{j\omega} . K_{div}$

Where: K_p = phase comparator gain in volts/radian.
K_F = filter gain in volts/volt.
K_{vco} = VCO conversion gain in radians/sec-volt.
K_{div} = divider gain in radians/radian (1/128).

Selection of the frequency at which the loop gain is unity (0dB) depends on the application, the unity gain frequency should be high enough to allow the loop to track expected variations of the reference frequency but low enough to provide a 'flywheel' action to average noise and unwanted input transients.

Some typical loop filter component values for the FX406 using phase comparator II are tabled below.

f_{ug} Unity gain frequency (Hz)	R_{17} = 1.8kΩ		C_{15} (F)
	R_{16} (Ω)	R_{15} (Ω)	
50	92k	13k	1μ
100	39k	6k2	1μ
250	200k	62k	0.1μ
500	16k	24k	0.1μ

When using phase comparator I, the loop filter frequency response may be used to limit the capture range of the loop, that is the range of input frequencies that the loop will lock onto. This property may be used to provide a degree of selectivity if required. The following table shows filter component values for various capture ranges. It should be noted that the loop filter used here is the simple 'lag' filter (i.e. $R_2 = 0$), this is to minimise ripple at 2 x f_{in} on the loop filter output which would cause frequency modulation of the switched capacitor filter response.

Capture Range $2f_c$ (Hz)	R_3 (Ω)	C_4 (F)
100	470k	340n
200	100k	390n
500	100k	68n
1000	100k	15n
2000	100k	3.9n

Note 3 — Phase Comparators

The following table shows the principal characteristics of second order loops using phase comparator I ('EX-OR') with a 'lag' filter and phase comparator II (edge-triggered) using a 'lead-lag' filter.

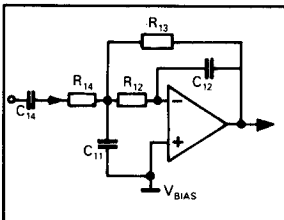
	PC I	PC II
Input duty cycle	50% optimum	don't care
Locks on harmonics of wanted signal	Yes	No
Noise rejection	Good	Poor
Ripple at 2 x f_{in} on loop filter output	Yes	Low
Lock range, $2f_l$	$f_{max} - f_{min}$	$f_{max} - f_{ug}$
Capture range, $2f_c$	$\frac{1}{\pi}\sqrt{\frac{K_p K_{vco} K_{div}\pi}{2\tau_1}}$	$f_{max} - f$
Frequency of VCO for no signal input	$\frac{f_{max} - f_{min}}{2}$	f_{min}
Phase angle between f_{ref} and $f_{vco}/128$ in lock.	0° at f_{min} 180° at f_{max} 90° at mid-point	0°

Note 4 — Anti-aliasing

The relationship between f_o and the switched capacitor sampling clock in the FX406 is $f_{clk} = 64f_o$. This type of sampled filter produces alias or image responses centred on half the sampling rate, i.e., $32f_o$,

Filters with passbands extending beyond $32f_o$ will have spurious responses reflected into the passband at a corresponding distance below $32f_o$.

If the input frequency spectrum to the filter is likely to contain components at these alias frequencies then an additional RC filter is required to attenuate these inputs. This is easily accomplished by using the filter input amplifier, Fig. 11 shows a 2nd order 5kHz lowpa filter with passband gain suitable for values of f_o above 250Hz.



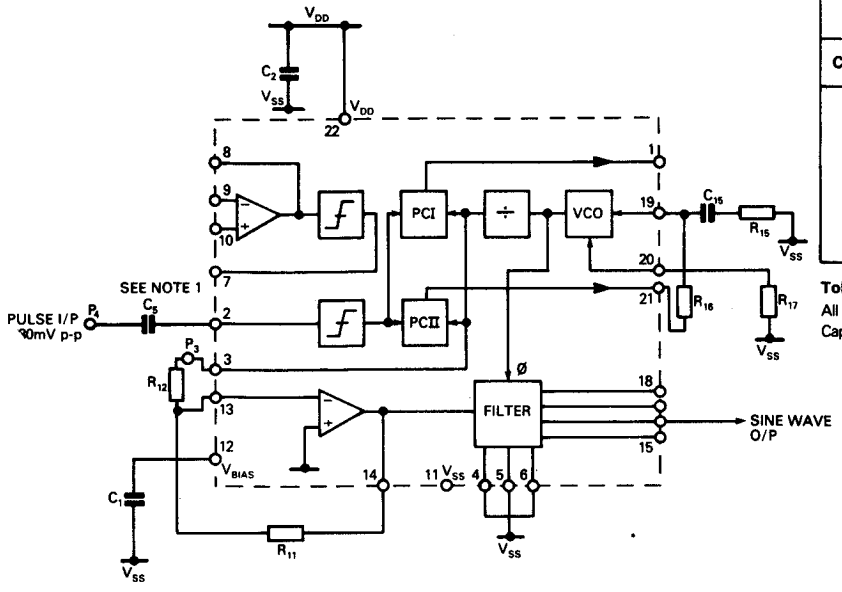
R_{12}	47kΩ
R_{13}	100kΩ
R_{14}	100kΩ
C_{11}	560pF
C_{12}	150pF
C_{14}	0.1μF

Fig. 11 Anti-Aliasing Filter

Special Note

Care must be taken when using the FX406 with f_o below 200Hz as the aliasing frequencies lie within the specified minimum passband of the filter.

On the highpass filter only, an additional lowpass response exists with its — 3dB point at $7f_c$ and a roll-off of 20dB/decade.

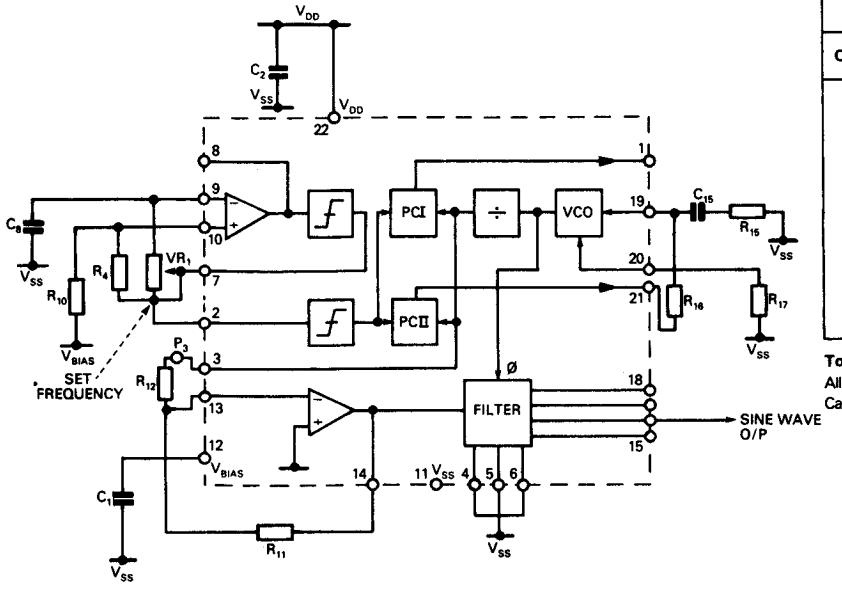


Component References	
Component	Unit Value
R_{11}	24k
R_{12}	330k
R_{16}	39k
R_{15}	6.2k
R_{17}	1.8k
C_1, C_2	1.0µ
C_5	0.1µ
C_{15}	1.0µ

Tolerance
All resistors ± 5%
Capacitors ± 20%

NOTE 1
C_5 can be omitted for TTL or CMOS logic level input signals.

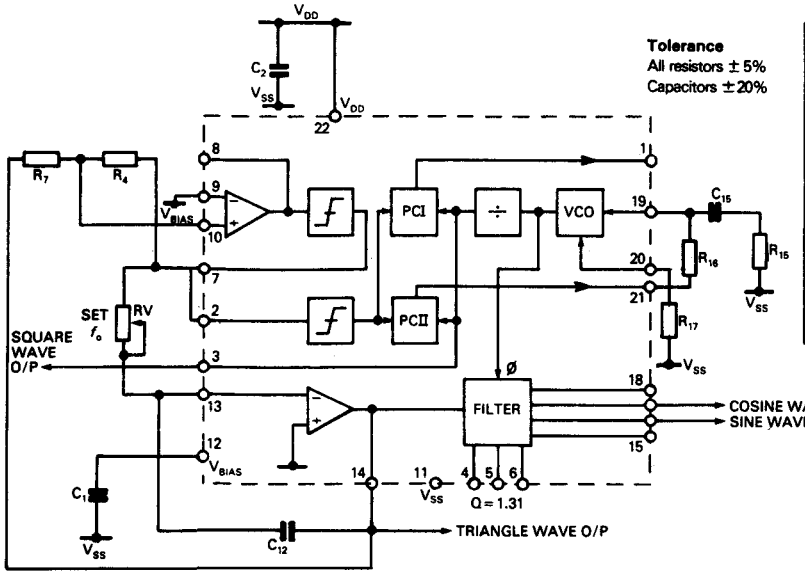
Fig. 12 Pulse to Sine Converter



Component References	
Component	Unit Value
R_4	200k
R_{10}	100k
R_{11}	24k
R_{12}	330k
R_{14}	220k
R_{15}	13k
R_{16}	91k
R_{17}	1.8k
C_1, C_2	1.0µ
C_8	4.7n
C_{15}	1.0µ
VR_1	1MΩ

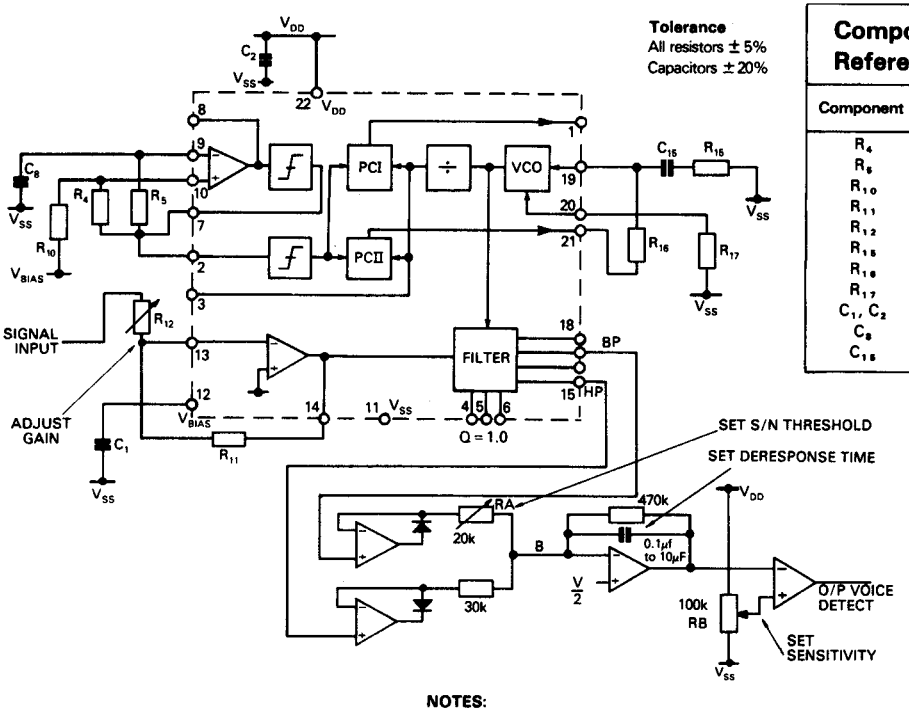
Tolerance
All resistors ± 5%
Capacitors ± 20%

Fig. 13 1kHz Sine Wave Oscillator



Component References	
Component	Unit Value
R_4	180k
R_7	100k
R_{15}	13k
R_{16}	91k
R_{17}	1.8k
RV	1M
C_1, C_2	1.0µ
C_{12}	4.7n
C_{15}	1.0µ

Fig. 14 Function Generator



Component References	
Component	Unit Value
R_4	100k
R_5	56k
R_{10}	100k
R_{11}	24k
R_{12}	30k
R_{15}	62k
R_{16}	200k
R_{17}	1.8k
C_1, C_2	1.0µ
C_8	10n
C_{15}	0.1µ

NOTES:
1. *Adjust gain R_{12} for largest filter output without clipping.*
2. *Vary R_A to give $V_{DD}/2$ at point B.*
3. *Set R_B for threshold.*
4. *Set C_A for de-response time.*

Fig. 15 Voice Operated Switch

Component References	
Component	Unit Value
R_4	100k
R_{10}	100k
R_{11}	24k
R_{12}	330k
R_{15}	24k
R_{16}	16k
R_{17}	1.8k
VR_1	100k
C_1, C_2	1.0µ
C_8	4.7n
C_{15}	0.1µ

Tolerance
All resistors ± 5%
Capacitors ± 20%

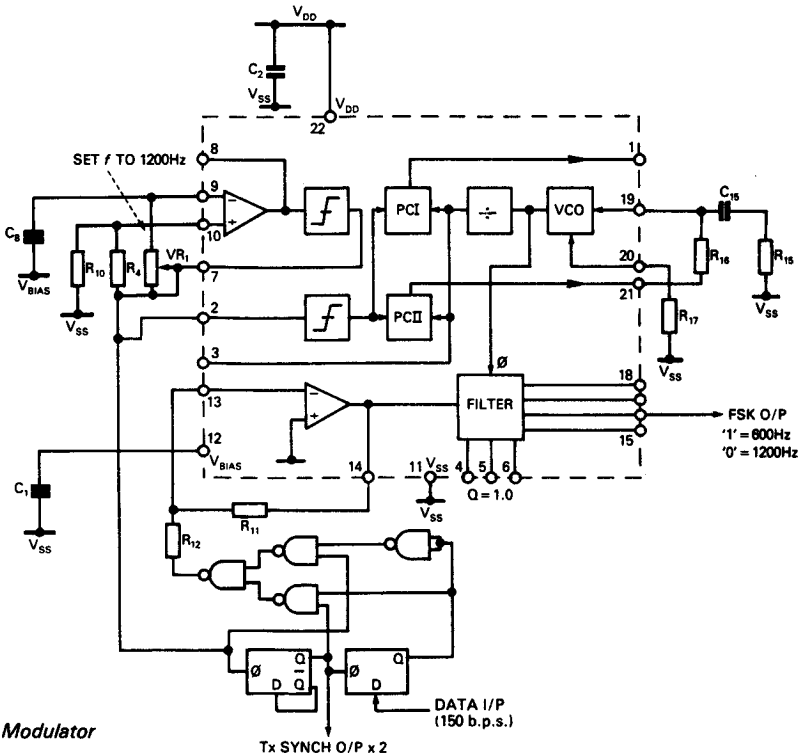


Fig. 16 150 Baud FSK Modulator

Component References	
Component	Unit Value
R_4	200k
R_{10}	130k
R_{11}	270k
R_{12}	24k
R_{17}	1.8k
VR_2	50k
C_1, C_2	1.0µ
C_{13}	0.1µ

Tolerance
All resistors ±5%
Capacitors ±20%

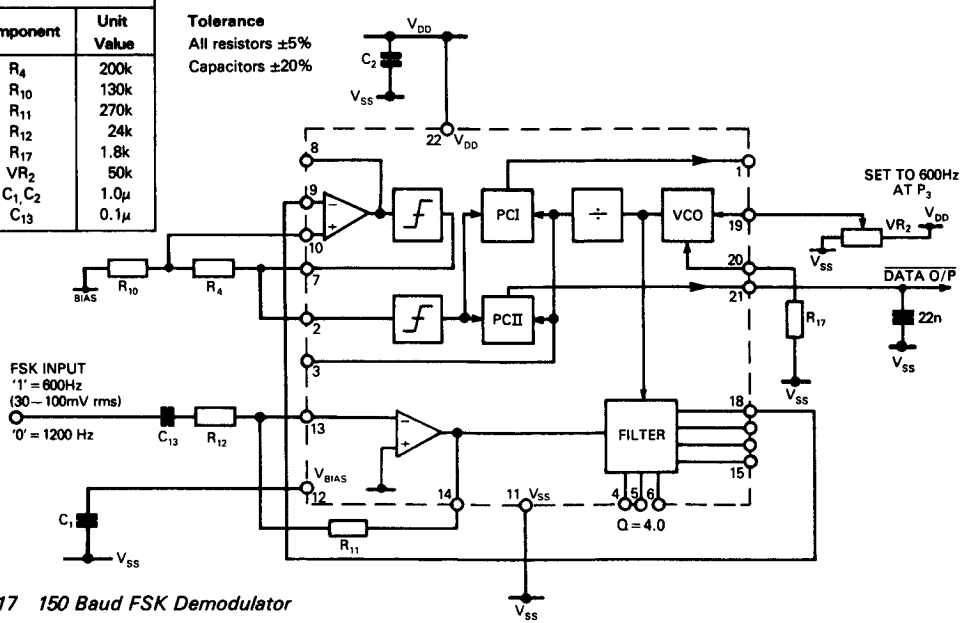


Fig. 17 150 Baud FSK Demodulator

Package Outlines

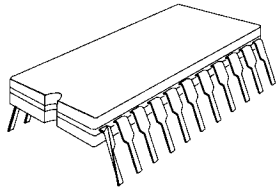
The FX406 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX406 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX406J 22-pin cerdip DIL (J3)

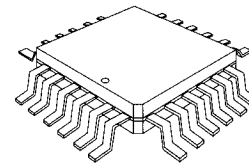
NOT TO SCALE



Max. Body Length 27.38mm
Max. Body Width 9.75mm

FX406LG 24-pin quad plastic encapsulated bent and cropped (L1)

NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

Ordering Information

FX406J 22-pin cerdip DIL (J3)

FX406LG 24-pin plastic encapsulated bent and cropped (L1)